IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Art Unit: 2661 Examiner: Phan, Tri H.

Serial No. 09/612,067 Filed: July 7, 2000

In Re Application of: Joel Naumann

For: METHOD AND APPARATUS FOR COMMUNICATION OF MISSING LOGIC IN A PCI BASED SYSTEM BY ENABLING OR DISABLING PCI CONFIG CYCLES

BRIEF ON APPEAL

Commissioner of Patents
Box AF
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Sirs:

This is a Brief on Appeal for consideration by the Board of Patent Appeals and Interferences ("Board") of the Final Office Action, dated June 05, 2006, rejecting all of the claims of the present application. A timely Notice of Appeal was filed on October 5, 2006.

REAL PARTY IN INTEREST

The only real party in interest regarding the present application is Cisco Technologies, Inc., assignee of the present application.

RELATED APPEALS AND INTERFERENCES

To the best of Appellants' knowledge, there are no appeals or interferences that will directly affect or be directly affected by or have a bearing upon the Board's decision in the pending appeal.

STATUS OF CLAIMS

There are a total of 19 claims (claims 1, 3, 5-10, 13-18, and 20-24) in the application. Claims 1, 3, 5-10, 13-18, and 20-24 have been rejected under 35 USC 103(a) as being unpatentable over (U.S. 5,923,663 to Bontemps). Claims 1, 3, 5-10, 13-18, and 20-24 are on appeal.

STATUS OF AMENDMENTS

There were no amendments filed subsequent to the Final Office Action.

SUMMARY OF THE INVENTION

The present invention relates to routers and switches and the detection and communication of a PHY level logic to a host processor. The first aspect of the present invention includes a front card configured to accept a Fast Ethernet device ona PCI-compliant bus, and the front card includes a switch that is serially disposed on a PCI_AD to device IDSEL connection corresponding to a particular channel on the front card. The switch is configur5ed to receive a sensing signal corresponding to the channel from the device. The switch is configur4ed to enable the connection of PCI_AD to FE MAC device IDSEL on the front card if the sensing signal is in a first state, and provide a low potential to the device's IDSEL input on the front card if the sensing signal is in a second state.

In a second aspect, the present invention comprises a switching means disposed on the front card; the switching means is configured to receive a sensing signal from the back card. The sensing signal has a first and a second state, and the switching means is

configured to provide a predetermined signal to the front card depending on the state of the sensing signal.

In a third aspect, the present invention provides a method comprising receiving, by the front card, a sensing signal from the back card; if the sensing signal is a logical low, then providing a PCI_AD to device IDSEL connection corresponding to a particular channel on the back card to the front card; if the sensing signal is not a logical low, then decoupling the PCI-AD to device IDSEL connection and providing a logical low signal in the place of the PCI_AD line.

GROUPING OF CLAIMS

Appellants consider that although all of the claims presented for consideration before the Board are allowable over the prior art of record, the patentability of individual claims may stand or fall as a group. Claims 1, 3 5-10, 13-18, and 20-24 are grouped. Claims 1, 3, and 5-9 are grouped. Claims 10, 13-17 are grouped. Claims 18, 20-24 are grouped.

ARGUMENT

1. The 35 USC 103(a) rejection

Regarding Examiner's rejection of claims 1, 3, 5-10, 13-18, and 20-24, Applicant submits that Bontemps, when combined with Applicant's admitted prior art (AAPA) does not disclose the limitations of claims 1, 3, 5-10, 13-18, and 20-24. Specifically, Examiner rejected independent claims 1, 10, and 18, by citing FIG. 1, elements 100 and 101 as teaching this same limitation. However, independent claims 1, 10, and 18 are directed to a router having a front card comprising an FE MAC, and a back card comprises an FE Phy. In stark comparison, element 100 in FIG. 1 refers to a computer network, and there

is no element 101 in Bontemps. Thus, the cited prior art does not teach or suggest all of the claim limitations.

In order to combine Bontemps with AAPA, the Examiner must show that Bontemps in combination with AAPA would arrive at Applicant's invention. Absent this, there is no motivation to combine Bontemps with AAPA because such combination doesn't solve the problem described in Applicant's AAPA.

In conclusion, Applicant respectfully submits that the 35 USC 103(a) rejection of claims 1, 10 and 18 as amended (and thus their respective dependent claims) cannot be sustained. If the Examiner feels there are any remaining issues that can be resolved by telephone, Examiner is invited to call the undersigned attorney at the phone number listed below.

Respectfully submitted,
SIERRA PATENT GROUP, LTD.

Date: December 4, 2006

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IN THE CLAIMS:

1. (Previously presented) In a communications system having a router, said router having a PCI-compliant front card, said front card being configured to accept a LAN or WAN compliant back card, a method for detecting the absence of a Phy Layer device on the back card and communicating said absence to the front card, said method comprising:

receiving, by a switching input of a tri-state buffer provided on the front card, a sensing signal from the back card;

if said sensing signal is a logical low, then coupling a IDSEL signal corresponding to a particular channel of said back card to said front card; and

if said sensing signal is not low, then decoupling said IDSEL signal from said front card and providing a logical low signal in the place of said IDSEL line, wherein said front card comprises an FE MAC, and said back card comprises an FE Phy.

2. (Canceled)

3. (Previously presented) The method of claim 1, wherein said tri-state buffer further has an input and an output, said input and output being serially disposed on a IDSEL line corresponding to a particular channel.

4. (Cancelled)

5. (Previously presented) The method of claim 1, wherein said front card and said back card are coupled via an MII bus.

6. (Previously presented) The method of claim 1, wherein said front card comprises an HDLC control, and said back card comprises a T1/E1 framer/line interface.

7. (Previously presented) The method of claim 6, wherein said front card and said back card are coupled via a TDM bus.

8. (Previously presented) The method of claim 1, wherein said front card comprises an ATM SAR, and said back card comprises an ATM Phy.

9. (Previously presented) The method of claim 8, wherein said front card and said back card are coupled via a Utopia bus.

10. (Previously presented) In a communications system having a router, said router having a PCI-compliant front card, said front card being configured to accept a LAN or WAN compliant back card, an apparatus for detecting the absence of a Phy Layer device on the back card and communicating said absence to the front card, said apparatus comprising:

means for switching disposed on the front card comprising a tri-state buffer wherein said tri-state buffer has an input, an output, and a switching input wherein said input and said output of said tri-state buffer being serially disposed on said front card and said switching input of said tri-state buffer is configured to be coupled to said back card, wherein said front card comprises an FE MAC, and said back card comprises an FE Phy;

said means for switching being configured to receive a sensing signal from the back card, said sensing signal having a first and second state;

said means for switching being further configured to provide a predetermined signal to said front card responsive to said state of sensing signal.

11. (Canceled)

12. (Cancelled)

13. (Currently amended) The apparatus of claim 10, wherein said front card and said back card are coupled via an MII bus.

14. (Original) The apparatus of claim 10, wherein said front card comprises an HDLC control, and said back card comprises a T1/E1 framer/line interface.

15. (Original) The apparatus of claim 14, wherein said front card and said back card are coupled via a TDM bus.

16. (Original) The apparatus of claim 10, wherein said front card comprises an ATM SAR, and said back card comprises an ATM Phy.

17. (Original) The apparatus of claim 16, wherein said front card and said back card are coupled via a Utopia bus.

18. (Previously presented) An apparatus for detecting the absence of a LAN or WAN compliant device, said apparatus comprising:

a PCI-compliant front card, said front card being configured to accept a LAN or WAN compliant back card wherein said front card comprises an FE MAC, and said back card comprises an FE Phy;

said front card further having a switch, said switch being a tri-state-buffer being serially disposed on a IDSEL connection corresponding to a particular channel on said front card, said switch being further configured to receive a sensing signal corresponding to said channel from said device by switching input of said tri-state buffer; and

wherein said apparatus is configured to couple said IDSEL connection to said front card if said sensing signal is in a first state, and provide a low potential to said front card if said sensing signal is in a second state.

19. (Cancelled)

20. (Original) The apparatus of claim 18, wherein said front card and said back card are coupled via an MII bus.

21. (Original) The apparatus of claim 20, wherein said front card comprises an HDLC control, and said back card comprises a T1/E1 framer/line interface.

22. (Original) The apparatus of claim 18, wherein said front card and said back card are coupled via a TDM bus.

23. (Previously presented) The apparatus of claim 20, wherein said front card comprises an ATM SAR, and said back card comprises an ATM Phy.

24. (Original) The apparatus of claim 18, wherein said front card and said back card are coupled via a Utopia bus.